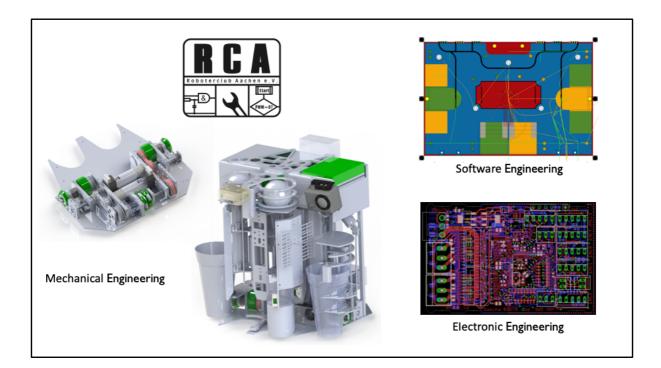
Improving Embedded Software with Data Science

Niklas Hauser

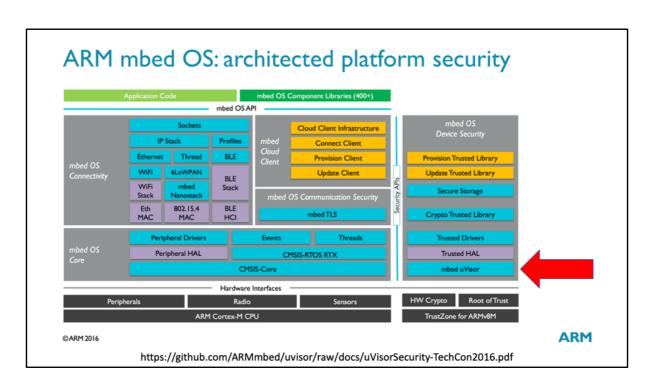
DLR Erfahrungsaustausch 2018



According to my parents I study something with computers.



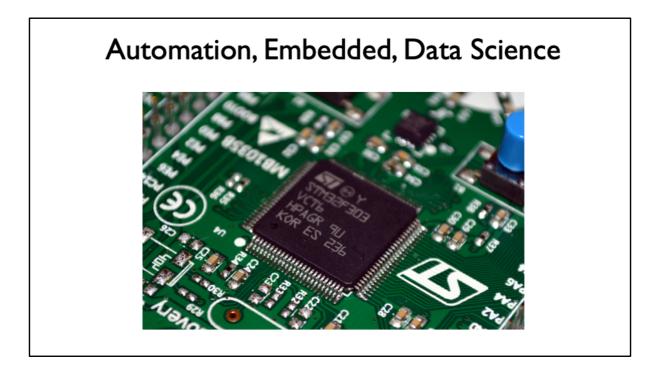
But I also build autonomous robots in my spare time.



2.5y ago, I got hired by ARM to work on mbed OS Security, specifically uVisor.I spent almost 2y on the lowest levels of the ARMv7-M and ARMv8-M architectures.I've seen ALL the dirt of Cortex-M and I still (mostly) love it.



Then I quit work to hack on the largest research model railway in Germany. YOLO.



This is an introduction talk, so I'll keep the technical details light and mostly talk about concepts and ideas.

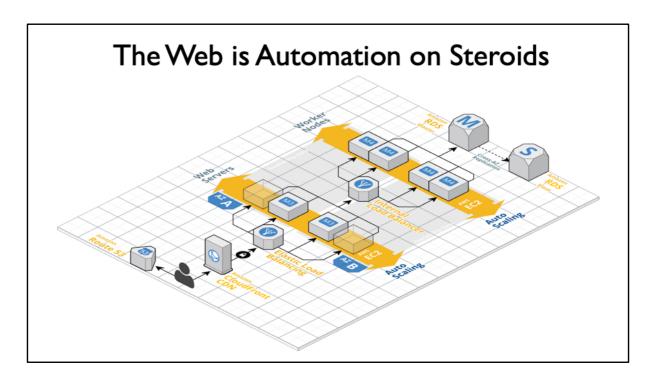
EMBEDDED: For the purpose of this talk I mean MICROCONTROLLERS, specifically AVR and ARM Cortex-M.



There many types of automation.

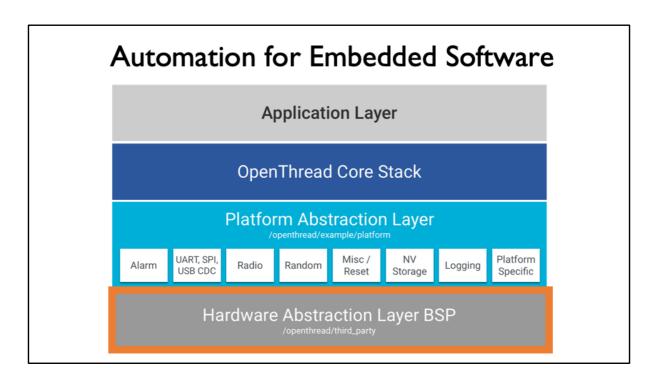
It evolved from a pure mechanization of labor to globe-spanning just-in-time industries.

This massive complexity only scaled with the introduction of computers.



The Web is the largest Automaton we've ever built! Everything you know about industrial automation, the Web does at >10x scale.

The key here is an asymmetry of effort: The developer configures the automation once, and then it just works[™].



What similar technology can I use for embedded software to get similar scaling benefits?

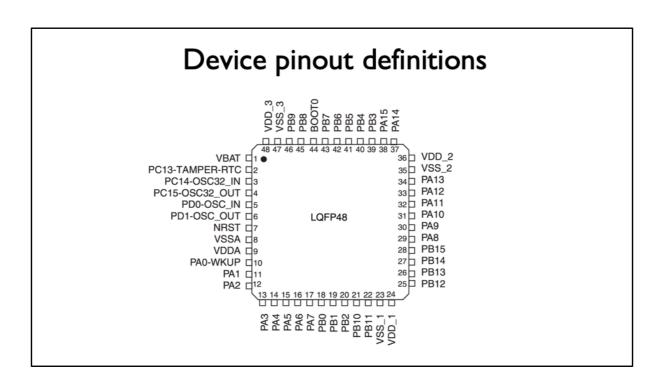
What needs to be scaled in embedded software? PORTING

HALs are usually provided by the vendor, to abstract hardware differences between devices.

USUALLY CODED BY HAND!

This is an insane BOTTLENECK.

PAL = Problem Anderer Leute

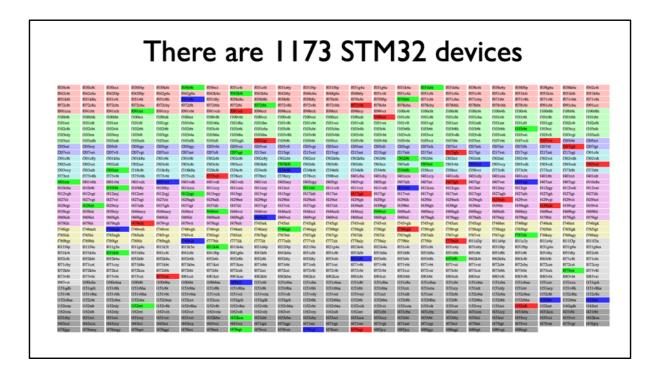


A typical abstraction of the HAL is to provide functions to access PINS. A single device can be packages in different ways, so the pins may differ.

Mbed OS is ported manually (!) // TIM4 cannot be used because already used by the us_ticker 86 87 MBED_WEAK const PinMap PinMap_PWM[] = { 88 {PA_1, PWM_2, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 2, 0)}, // TIM2_CH2 - Default {PA_2, PWM_2, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 3, 0)}, // TIM2_CH3 - Default (warning: not connected 89 {PA_3, PWM_2, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 4, 0)}, // TIM2_CH4 - Default (warning: not connected 90 91 {PA_6, PWM_3, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 1, 0)}, // TIM3_CH1 - Default {PA_7, PWM_3, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 2, 0)}, // TIM3_CH2 - Default 92 93 // {PA_7, FWM_1, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 6, 1, 1)}, // TIM1_CH1N - GPI0_PartialRemap_TIM1 {PA_8, PWM_1, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 1, 0)}, // TIM1_CH1 - Default 94 95 {PA_9, PWM_1, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPIO_PULLUP, 0, 2, 0)}, // TIM1_CH2 - Default {PA_10, PWM_1, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 3, 0)}, // TIM1_CH3 - Default 96 97 {PA_11, PWM_1, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPIO_PULLUP, 0, 4, 0)}, // TIM1_CH4 - Default 98 {PA_15, PWM_2, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 8, 1, 0)}, // TIM2_CH1_ETR - GPI0_FullRemap_TIM2 90 {PB_0, PWM_3, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 3, 0)}, // TIM3_CH3 - Default 100 101 // {PB_0, PWM_1, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 6, 2, 1)}, // TIM1_CH2N - GPI0_PartialRemap_TIM1 {PB_1, PWM_3, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 4, 0)}, // TIM3_CH4 - Default 102 103 // {PB_1, PWM_1, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 6, 3, 1)}, // TIM1_CH3N - GPI0_PartialRemap_TIM1 {PB_3, PWM_2, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 8, 2, 0)}, // TIM2_CH2 - GPI0_FullRemap_TIM2 104 105 {PB_4, PWM_3, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 7, 1, 0)}, // TIM3_CH1 - GPI0_PartialRemap_TIM3 {PB_5, PWM_3, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 7, 2, 0)}, // TIM3_CH2 - GPI0_PartialRemap_TIM3 106 107 // {PB_6, PWM_4, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 1, 0)}, // TIM4_CH1 - Default (used by ticker) // {PB_7, PWM_4, STM_PIN_DATA_EXT(STM_MODE_AF_PP, GPI0_PULLUP, 0, 2, 0)}, // TIM4_CH2 - Default (used by ticker) 108

In mbed OS this table describes the pin signal connections to the internal peripherals. You can see some manually commented out lines.

ST has 4-6 full-time engineers just for porting Mbed OS to STM32. They do it completely by hand.



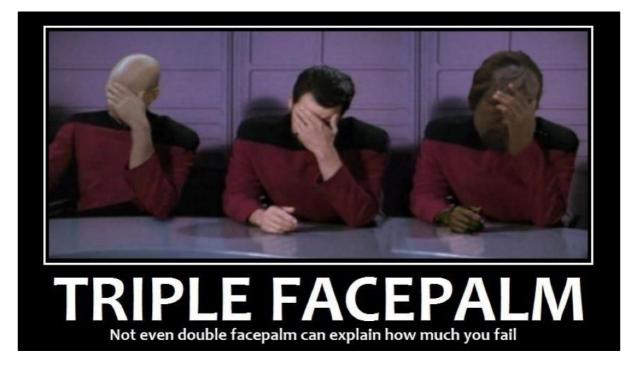
ST adds new devices every couple of months.

Most of them differ in memory size, package and peripherals.

Mbed OS supports 55 STM32 devices

\$ find targets/TARGET_STM -name "PeripheralPins.c" targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/PeripheralPins.c targets /TARGET STM/TARGET STM32F0/TARGET NUCLED F030R8/ParinharalPine (targe \$ find . -name "STM32*.ld" targe /targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/TOOLCHAIN_GCC_ARM/STM32F0xx.ld targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_GCC_ARM/STM32F0xx.ld
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F030R8/device/T00LCHAIN_GCC_ARM/STM32F030X8.ld
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_ARM_MICRO/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_ARM_MICRO/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_ARM_MICRO/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_ARM_MICRO/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_ARM_STD/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_ARM_STD/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_GCC_ARM/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_GCC_ARM/startup_stm32f05
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targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_GCC_ARM/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_STM32F0/TARGET_DISCO_F051R8/device/T00LCHAIN_GCC_ARM/startup_stm32f05
targe:/targets/TARGET_STM/TARGET_STM32F0/TARGET_STM32F targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLE0_F030R8/device/TOOLCHAIN_ARM_MICR0/startup_stm32 targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLE0_F030R8/device/TOOLCHAIN_ARM_STD/startup_stm32f0 targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F030R8/device/TOOLCHAIN_GCC_ARM/startup_stm32f targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLE0_F030R8/device/T00LCHAIN_IAR/startup_stm32f030x8 targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLE0_F031K6/device/T00LCHAIN_ARM_MICR0/startup_stm32 targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F031K6/device/T00LCHAIN_ARM_STD/startup_stm32f0 targe./targe targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F031K6/device/T00LCHAIN_IAR/startup_stm32f031x targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F042K6/device/TOOLCHAIN_ARM_MICRO/startup_stm32 targe./targe./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLE0_F042K6/device/T00LCHAIN_ARM_STD/startup_stm32f0 targe./targe /targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F042K6/device/T00LCHAIN_GCC_ARM/startup_stm32f0
targe /targe /target/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F042K6/device/T00LCHAIN_GCC_ARM/startup_stm32f0 targe./targe
/targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F042K6/device/T00LCHAIN_GCC_AKM/startup_stm32f042x6
targe./targe /targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLEO_F042K6/device/T00LCHAIN_IAR/startup_stm32f042x6 ./targets/TARGET_STM/TARGET_STM32F0/TARGET_NUCLE0_F070RB/device/T00LCHAIN_ARM_MICR0/startup_stm32

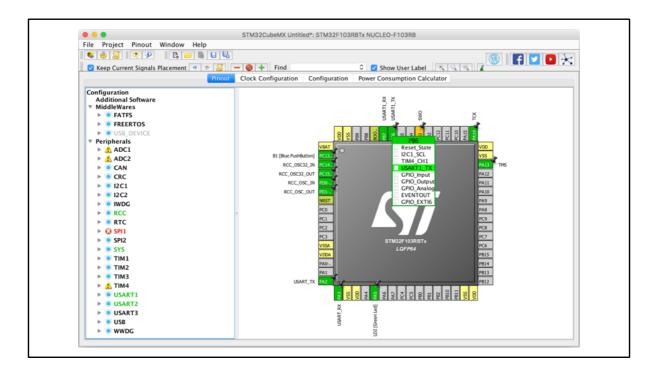
- 55 manually created versions of the pinout data
- 51 Linkerscripts (some manually patched)
- ~200 startup scripts (some manually patched)
- We needed to modify the linker- and startup script for uVisor



X Billion IoT devices by 2035? HOW ARE YOU GOING TO MAINTAIN THIS?!?



Let's think about this problem in a calm and structured manner. Tea?



STMicro publishes a GUI App to initialize your STM32.

It's pretty good, the usability of this is great, you can just visually configure all your pins.

Understand conflicts between peripheral signal connections etc.

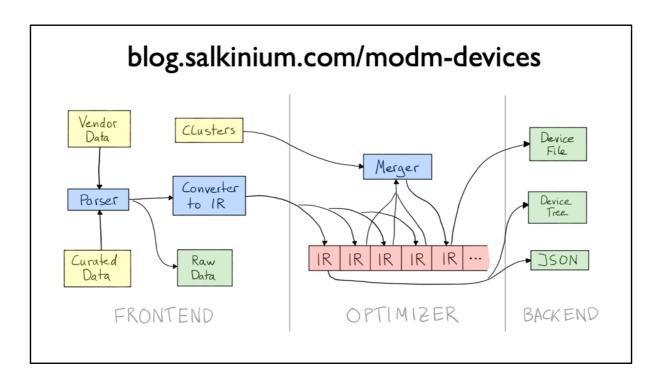
But I got curious, how does this work? It's backed by a lot of DATA!

STM327103V8-80%xml STM327103V8-80%xml STM327103V8-7-60%xml STM327103V8-7-60%xml STM327103V8-6-70%xml STM327103V8-7-67%xml STM327103V8-70%xml STM327103V8-70%xml STM32710105-80%xml STM327103V8-70%xml STM327103V8-70%xml STM327103V8-70%xml STM32710105-70%xml STM327103V8-70%xml STM327103V8-70%xml STM327103V8-70%xml STM32710105-70%xml STM32710105-70%xml STM32710105-70%xml STM32710105-70%xml STM32710105-70%xml STM32710105-70%xml STM32710705-70%xml STM32710105-70%xml STM32710105-70%xml STM32710105-70%xml STM32710705-70%xml STM32710705-70%xml STM32710105-70%xml STM32710706-70%xml STM32710706-70%xml STM32710706-70%xml STM327107070-70%xml STM32710706-70%xml STM32710706-70%xml STM32710706-70%xml STM327107070-70%xml STM32710706-70%xml STM32710706-70%xml STM32710706-70%xml STM327107070-70%xml STM32710706-70%xml STM32710706-	ce Files
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70MB of XML files, with a lot of device details.



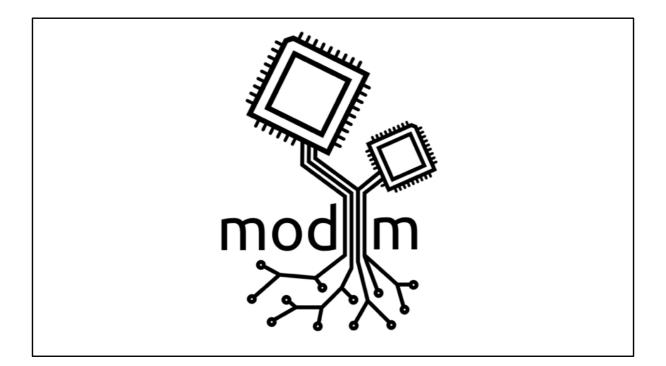
- CPU: Type and Interrupt Vector Table
- Memories: Flash, RAM, Backup
- Peripherals: Type and Instances
- Gpio: Name and Signals



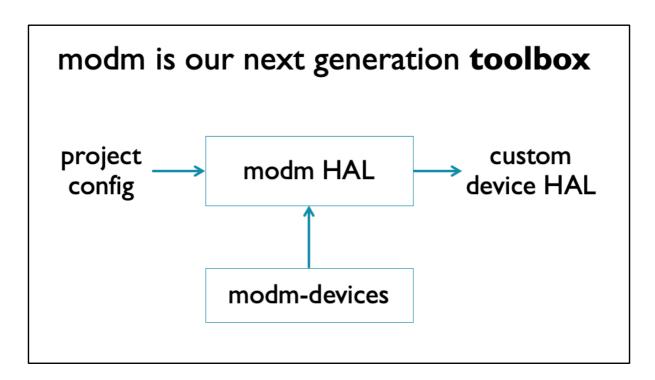
The reality is a bit more involved.

~	200 STM3	32s +	~ 200 A	VRs
📮 modm-io / modm-d	evices		⊙ Unwatch - 5	tunstar 7 ∛Fork 1
<> Code (1) Issues (0)	아 Pull requests 이 네 In	sights 🔅 Settings		
	all AVR and STM32 devices ht nicrocontroller device-tree mod	ttp://blog.salkinium.com dm Manage topics	n/modm-devices	Edit
74 commits	β 3 branches	♥ 0 releases	2 contributors	ಫೆ MPL-2.0
	₽ 3 branches	♡ O releases	2 contributors Create new file Upload files	화 MPL-2.0 Find file Clone or download ◄
Branch: develop - New p	0	♥ 0 releases	Create new file Upload files	
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Branch: develop - New p	header-stm32 submodule	device files.	Create new file Upload files	Find file Clone or download ✓ Latest commit dd631c0 7 days ago 3 months ago
Branch: develop New p Salkinium Update cmsis- devices	header-stm32 submodule	device files.	Create new file Upload files	Find file Clone or download ★ Latest commit dd631c0 7 days ago 3 months ago 7 days ago
Branch: develop New p Salkinium Update cmsis- devices tools	header-stm32 submodule Update STM32 and AVR of Update cmsis-header-str	device files. m32 submodule	Create new file Upload files	Find file Clone or download -

YOU can use this data too, it's on GitHub

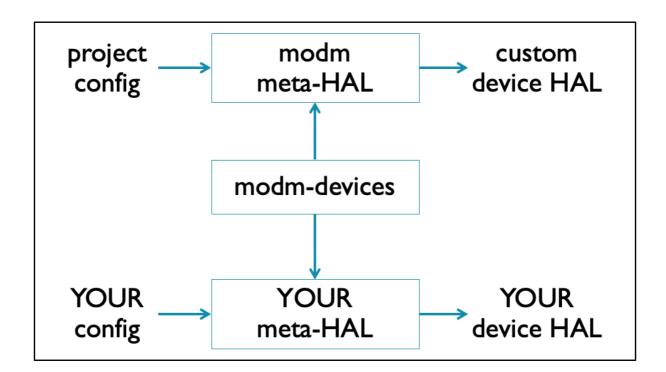


Fabian and I worked on modm for the last two years. It's a C++ HAL for STM32 and AVR. We use it to build the robot software for the Roboterclub Aachen.



modm is our INTERPRETATION of modm-devices.

It's a library GENERATOR, we specify a target id and it generates the HAL for us. We have ported ~80 AVRs and ~850 STM32 so far.



Share the data, not the HAL.

Easier to customize your HAL to your specific needs.

THIS IS LANGUAGE INDEPENDENT!

You generate C, Go, Rust, TEXT, you can also just generate documentation.

You can generate just ONE file, then gradually expand. Particularly useful to replace pain-points in existing code bases.

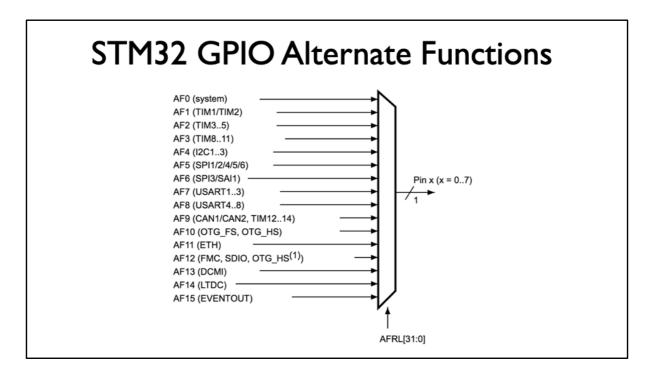
Vertical vs. Horizontal Porting											
Feature	STM32F0	STM32FI	STM32F3	STM32F4	STM32F						
Core	✓	\checkmark	V	\checkmark	~						
GPIO	✓	√	V	\checkmark	V						
Clock	✓	v	v	√	v						
UART	✓	V	V	√	V						
SPI	VV	VV	V V	V V	×.						

There is a change in how you port your targets now: Before: For each target implement the feature. Now: for each feature port to all targets



I glossed over the details of the actual code generation. You can read up on this on our website with examples. Installation guide, getting started guide, explanations how it works.

I'm not here to sell you on our HAL, I want to show you specific problems and how we used our toolbox to solve them.



I've already touched on signal connections.

Each pin has a number of peripherals that it can be connected to.

															1		
		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
Por	Port	SYS	TIM1/2	TIM3/4/ 5	TIM8/9/ 10/11	I2C1/2/3	SPI1/2/3 /4/5/6	SPI2/3/ SAI1	SPI2/3/ USART 1/2/3	USAR T6/UA RT4/5 /7/8	CAN1/2/ TIM12/1 3/14/QU ADSPI/L CD	QUAD SPI/OT G2_HS /OTG1 _FS	ETH	FMC/SD IO/OTG2 _FS	DCMI/ DSI HOST	LCD	SYS
	PA0		TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR				USART2_ CTS	UART4_ TX			ETH_MII_CRS				EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-		-	USART2_ RTS	UART4_ RX	QUADSPI_ BK1_IO3	-	ETH_MII_RX_ CLK/ETH_RMI I_REF_CLK	-	-	LCD_R2	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_T X	-	•	-	ETH_MDIO	-	-	LCD_R1	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	•	-	USART2_ RX	-	LCD_B2	OTG_HS _ULPI_D0	ETH_MILCOL	-	-	LCD_B5	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS/ I2S3_WS	USART2_ CK	-		-	-	OTG_HS_S OF	DCMI_HS YNC	LCD_VSY NC	EVENT OUT
	PA5	-	TIM2_CH1/ TIM2_ETR		TIM8_CH1 N	-	SPI1_SCK	-		-		OTG_HS _ULPI_C K	-			LCD_R4	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKI N	-	SPI1_ MISO	-	-	-	TIM13_CH1		-		DCMI_PIX CLK	LCD_G2	EVENT OUT
Port	A PA7	-	TIM1_ CH1N	TIM3_CH2	TIM8_CH1 N	-	SPI1_ MOSI	-	-	-	TIM14_CH1	QUADSPI _CLK	ETH_MII_RX_ DV/ETH_RMII _CRS_DV	FMC_SDN WE	-	-	EVENT OUT
	PA8	MCO1	TIM1_CH1	-	-	I2C3_SCL		-	USART1_ CK	-	•	OTG_FS_ SOF	-	-	-	LCD_R6	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_SMBA	SPI2_SCK/I 2S2_CK	-	USART1_T X	-	-	-	-	-	DCMI_D0	-	EVENT OUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_ RX	-	-	OTG_FS_ ID	-	-	DCMI_D1	-	EVENT OUT
	PA11	-	TIM1_CH4	-	-	-		-	USART1_ CTS	-	CAN1_RX	OTG_FS_ DM		-		LCD_R4	EVENT OUT
	PA12	-	TIM1_ETR	-	-	-		-	USART1_ RTS	-	CAN1_TX	OTG_FS_ DP		-		LCD_R5	EVENT OUT
	PA13	JTMS- SWDIO	-	-	-	-	-	-	-	-		-		-	-	-	EVENT OUT
	PA14	JTCK- SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-		SPI1_NSS	SPI3_NSS/ I2S3_WS	-	-	-	-	-	-	-	-	EVENT 'OUT

These connections are hardcoded, and the possibilities are described in a very long table in the datasheet.

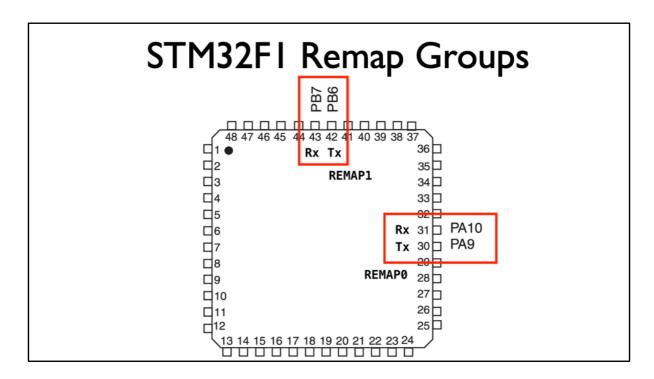
Several pages of tables.

You do NOT want to read through that.

Gpio Signal Connection API GpioB7::connect(Uart1); GpioB6::connect(Uart1); But this code breaks RX on PB7! GpioB7::connect(Uart1); GpioA9::connect(Uart1);

We came up with this API. Just connect the pin to the peripheral.

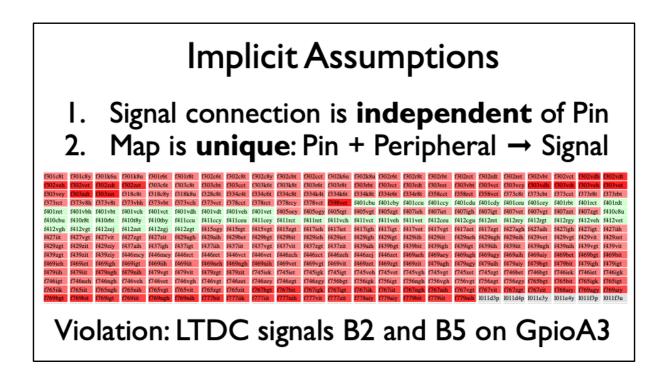
Worked fine for a long time, until we ported to STM32F1! Things suddenly broke.



On the STM32F1 the GPIOs can only remap in groups. NO INDIVIDUAL REMAP POSSIBLE!

Our API has side-effects and the last call to set the group wins. This is an implicit assumption of our HAL API: Signal connections are independent of each other!

It's FALSE.

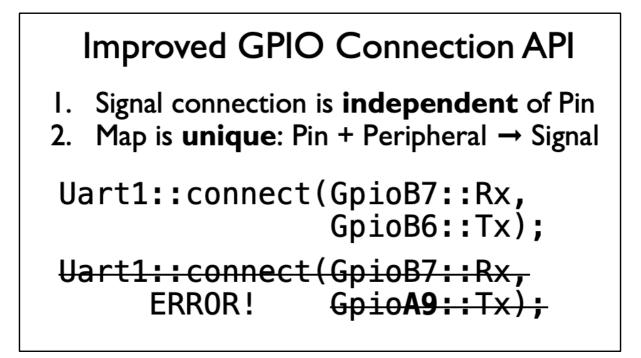


There is another assumption:

The combination of Pin NAME and Peripheral NAME is enough to **uniquely** identify the Signal connections.

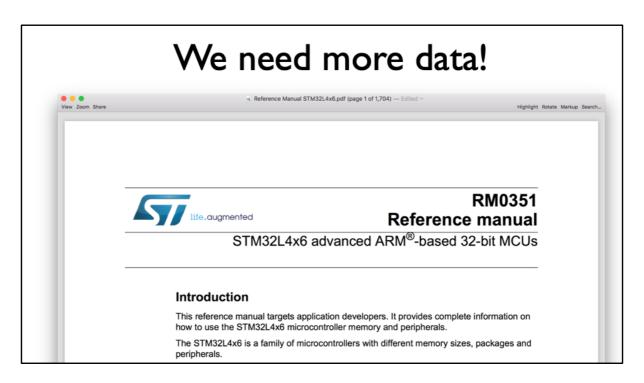
So we wrote these assumptions as a test and ran it over all devices. Shows about 400 devices, the more red, the more violations.

An example violation: LCD display peripheral signals map two Blue signal lines onto the same pin.



So we changed our API. Broke the entire code. And this API now remaps both in a group.

Compiler checks group remap validity.



The CubeMX data doesn't contain everything we want. And it also doesn't scale to other vendors. So let's have a look at a very verbose data source: THE REFERENCE MANUALS.

Let's parse some PDFs Table 39. Summary of the DMA1 requests for each channel										
Request. number	- ' Channel 1 Channel 2 Channel 3 Channel 4 Channel 5 Channel 6 Channel									
0	ADC1	ADC2	ADC3	DFSDM1_ FLT0	DFSDM1_ FLT1	DFSDM1_ FLT2	DFSDM1_ FLT3			
1	-	SPI1_RX	SPI1_TX	SPI2_RX	SPI2_TX	SAI2_A	SAI2_B			
2	-	USART3_TX	USART3_RX	USART1_TX	USART1_RX	USART2_RX	USART2_TX			
3	-	I2C3_TX	I2C3_RX	I2C2_TX	I2C2_RX	I2C1_TX	I2C1_RX			

This is a DMA channel to peripheral mapping.

This is data that's not available in the CubeMX dataset.

We need it anyways to provide a channel connection API.

PDF X-Ray Vision											
Reguest. number	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7				
٥	ADC1	ADC2	ADC3	DESDM1_ FLITO	DESDM1_ ELTI	DESDM1_ FLIT2	DESDM1_ ELIT3				
đ	-	SPI1_RX	SPI1_IIX	SPI2_RX	SPI2_TIX	SAI2_A	SAI2_B				
2	-	USART3_TX	USART3_RX	USARTI1_TIX	USARTI1_RX	USART2_RX	USART2_TX				
3	-	I2C3_IIX	I2C3_RX	12C2_TX	12C2_RX	12C1_TX	I2C1_RX				

I wrote a program to give me X-Ray vision of the PDF. Read the Adobe PDF specification, it's quite fun.

PDF is a print format, it does not contain any semantical intofmraiton. This is not a table. It is a bunch of lines and a bunch of text overlaid.

You can recognize tables fairly easily, and then translate their contents.

Table extraction is doable

Re- quest. num- ber	Chan nel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7
0	ADC1	ADC2	ADC3	DFSD- M1_FLT0	DFSD- M1_FLT1	DFSD- M1_FLT2	DFSD- M1_FLT3
1	-	SPI1_RX	SPI1_TX	SPI2_RX	SPI2_TX	SAI2_A	SAI2_B
2	-	USAR- T3_TX	USAR- T3_RX	USART1_T X	USART1_R X	USART2_R X	USART2_T X
3	-	I2C3_TX	I2C3_RX	I2C2_TX	I2C2_RX	I2C1_TX	I2C1_RX

Understanding descriptions is very hard

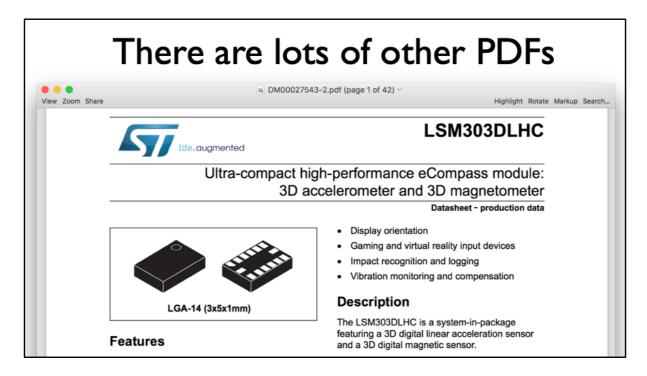
This is a prototype extraction. Tables are structured information by definition. So it's somewhat easy to extract and use this data.

However, the textual descriptions of periphrals are very hard to turn into some kind of structured information.

The difficulty is not the table extraction it's the data cleanup and simplification. You need to condense this information into something that easily usable for the developer.

There are hundreds of these datasheets + reference manuals. This isn't easy.

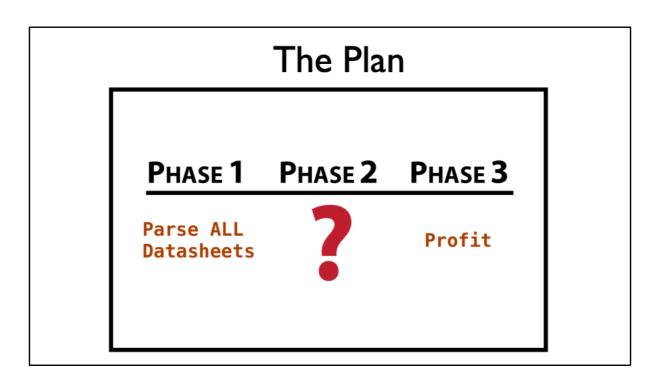
There are bugs in them, sometimes types in register names, sometimes worse. It's going to be difficult to get some ground truth out of this.



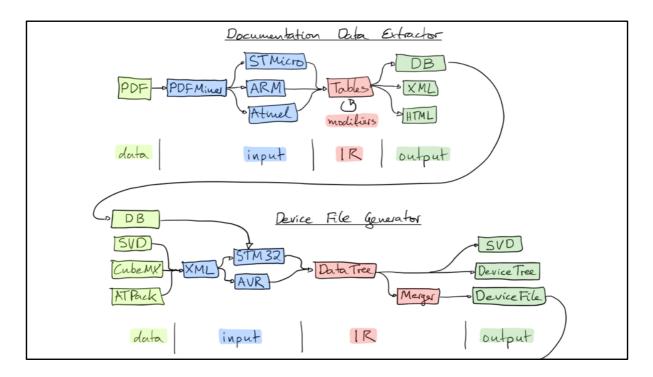
ST also produces SENSORS, which also have Datasheets. They have the same formatting as the reference manuals, so you can just extract tables in there too.

And so we can build a database of sensors as well. They are always the same: Memory Mapped IO via SPI/I2C.

They are by definition already platform-independent. So why aren't there COMMON drivers for all platforms? Abstract description of the protocol



This is really self-explanatory.



This is how I envision the future of Porting Embedded Software to hundreds of devices.

We parse ALL of the datasheets, THEN MAGIC, THEN PROFIT.

Thank you for listening!

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EY MANN, WO IS' MEIN TSCHUNK?